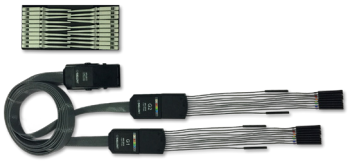
Logic Probe

Parameter / Model	SPL2016	Parameter / Model	SPL1016
			
Channels	16	Channels	16
Input Impedance	100 KΩ||18 PF	Input Impedance	100 KΩ||8 pF
Max. Input Voltage	±50 V peak	Max. Input Voltage	±20 V peak
Threshold Groupings	Pod 2: D15-D8 Pod 1: D7-D0	Threshold Groupings	Pod 2: D15-D8 Pod 1: D7-D0
Threshold Selections	TTL (1.5 V), COMS (2.5 V) , 3.3 V_LVCOMS (1.65 V), 2.5 V_LVCOS (1.25 V)	Threshold Selections	TTL (1.5 V), COMS (2.5 V), 3.3 V_LVCOMS (1.65 V), 2.5 V_LVCOS (1.25 V)
User defined threshold range	±3 V in 10 mv steps	User defined threshold range	±3 V in 10 mv steps
Threshold Accuracy	± (3%*Threshold+200 mv)	Threshold Accuracy	± (3%*Threshold+150 mv)
Input Dynamic Range	±20 V	Input Dynamic Range	±10 V
Min. Input Voltage Swing	800 mVp	Min. Input Voltage Swing	800 mVpp
Max. Input Frequency	Probe: 150 MHz Line: 50 MHz	Max. Input Frequency	60 MHz
Min. Detectable Pulse Width	3.3 ns	Min. Detectable Pulse Width	8.3 ns
Channel Skew	±(1 digital sample interval)	Channel Skew	±(1 digital sample interval)

Parameter / Model	SPL1008
Channels	8
Input Impedance	100 KΩ||18 PF
Working Voltage	±5 Vpp
Non-destructive Voltage	±40 Vpp
User defined threshold range	-3 V~3 V
Threshold Selections	TTL (1.5 V), COMS (1.65 V), 3.3 V_LVCOMS (1.65 V), 2.5 V_LVCOS (1.25 V)
Threshold Accuracy	±400 mV
Delay Window	600 mVpp
Min. Input Voltage Swing	800 mVpp
Input level Limit	TTL (0 V≤VL≤0.8 V;2.4 V≤VH≤5 V) CMOS (0 V≤VL≤1.5 V;3.5 V≤VH≤5 V) 3.3 V_LVCOMS (0 V≤VL≤0.7 V;2 V≤VH≤3.3 V) 2.5 V_LVCOMS (0 V≤VL≤0.7 V;1.7 V≤VH≤2.5 V)
Cable length	80 CM±2 CM
Max. Data rate	120 Mbps
Timing sampling rate	500 Mbps
Status sampling rate	60 Mbps
Minimum input slew rate	75 mV/μS
Plus Width Resolution	TTL: 15 nS CMOS: 15 nS LVCMOS 3.3V: 15 nS